What is claimed is:

1. A buffer circuit comprising;

an output terminal;

a pull-up transistor connected between the output terminal and a supply voltage, wherein the pull-up transistor pulls the output terminal up to the supply voltage responsive to a pull-up control signal;

a pull-down transistor connected between the output terminal and a reference voltage, wherein the pull-down transistor pulls the output terminal down to the reference voltage responsive to a pull-down control signal;

a first logic gate configured to generate the pull-up control signal at a first output node responsive to a control signal and a data signal, and wherein the first logic gate includes a plurality of serially connected transistors in an electrical path between the supply voltage and the first output node; and

a second logic gate configured to generate the pull-down control signal at a second output node responsive to the data signal and an inverse of the control signal and wherein the second logic gate includes a plurality of serially connected transistors in a path between the supply voltage and the second output node;

wherein the number of serially connected transistors in the path between the supply voltage and the first output node is equivalent to the number of serially connected transistors in the path between the supply voltage and the second output node.

2. A buffer circuit according to Claim 1 wherein the plurality of serially connected transistors in the electrical path between the supply voltage and the first output node comprises a first transistor having a first control electrode connected to the data signal and a second transistor coupled in series between the supply voltage and the first transistor, the first logic gate further comprising a third transistor connected in parallel with the first transistor between the second transistor and the first output node, wherein the third transistor has a third control electrode connected to the

control signal.

3. A buffer circuit according to Claim 2 wherein each of the first, second, and third transistors have a same conductivity type.

4. A buffer circuit according to Claim 2 wherein the first transistor is a first PMOS transistor, wherein the second transistor is a second PMOS transistor, and wherein the third transistor is a third PMOS transistor.

5. A buffer circuit according to Claim 4 wherein the plurality of serially connected transistors in the path between the supply voltage and the second output node are PMOS transistors.

6. A buffer circuit according to Claim 4, the first logic gate further comprising a plurality of serially connected NMOS transistors between the first output node and the reference voltage, the plurality of serially connected NMOS transistors including a first NMOS transistor having a first NMOS control electrode connected to the data signal and a second NMOS transistor having a second NMOS control electrode connected to the control signal.

7. A buffer circuit according to Claim 6, the first logic gate further comprising a third NMOS transistor connected with the first output node, the third NMOS transistor having a third NMOS control electrode connected to the reference voltage.

8. A buffer circuit according to Claim 2 wherein the first and second logic gates are further responsive to a second control signal, the first logic gate further comprising a fourth transistor connected in parallel with the first and third transistors between the second transistor and the first output node, the fourth transistor having a control electrode connected

to the second control signal.

9. A buffer circuit according to Claim 8, the first logic gate further comprising a fifth transistor connected in series with the second transistor between the first transistor and the supply voltage.

10. A buffer circuit according to Claim 1 wherein the reference voltage comprises a ground voltage.

11. A buffer circuit according to Claim 1 wherein the first logic gate comprises a NAND gate and wherein the second logic gate comprises a NOR gate.

12. A buffer circuit according to Claim 1 wherein the plurality of serially connected transistors in the path between the supply voltage and the first output node are PMOS transistors, and wherein the plurality of serially connected transistors in the path between the supply voltage and the second output node are PMOS transistors.

13. An output buffer comprising;

an output terminal;

a pull-up transistor connected between the output terminal and a supply voltage, wherein the pull-up transistor pulls the output terminal up to the supply voltage responsive to a pull-up control signal;

a pull-down transistor connected between the output terminal and a reference voltage, wherein the pull-down transistor pulls the output terminal down to the reference voltage responsive to a pull-down control signal;

a first logic gate configured to generate the pull-up control signal at a first output node responsive to a control signal and a data signal, and wherein the first logic gate includes a plurality of serially connected transistors in a path between the first output node and the reference voltage; and

a second logic gate configured to generate the pull-down control signal at a second output node responsive to the data signal and an inverse of the control signal and wherein the second logic gate includes a plurality of serially connected transistors in a path between the second output node and the reference voltage;

wherein the number of serially connected transistors in the path between the first output node and the reference voltage is equivalent to the number of serially connected transistors in the path between the second output node and the reference voltage.

14. A buffer circuit according to Claim 13 wherein the plurality of serially connected transistors in the electrical path between the second output node and the reference voltage comprises a first transistor having a first control electrode connected to the data signal and a second transistor connected in series between the first transistor and the reference voltage, the second logic gate further comprising a third transistor connected in parallel with the first transistor between the second transistor and the second output node, wherein the third transistor has a control electrode connected to the inverse of the control signal.

15. A buffer circuit according to Claim 14 wherein each of the first, second and third transistors have a same conductivity type.

16. A buffer circuit according to Claim 14 wherein the first transistor is a first NMOS transistor, wherein the second transistor is a second NMOS transistor, and wherein the third transistor is a third NMOS transistor.

17. A buffer circuit according to Claim 16 wherein the plurality of serially connected transistors in the path between the first output node and the reference voltage are NMOS transistors.

18. A buffer circuit according to Claim 16, the second logic gate further comprising a plurality of serially connected PMOS transistors between the supply voltage and the second output node, the plurality of serially connected PMOS transistors including a first PMOS transistor having a first PMOS control electrode connected to the data signal and a second PMOS transistor having a second PMOS control electrode connected to the inverse of the control signal.

19. A buffer circuit according to Claim 18, the second logic gate further comprising a third PMOS transistor connected with the second output node, the third PMOS transistor having a third PMOS control electrode connected to the supply voltage.

20. A buffer circuit according to Claim 14 wherein the first and second logic gates are further responsive to a second control signal, the second logic gate further comprising a fourth transistor connected in parallel with the first and third transistors between the second transistor and the second output node, the fourth transistor having a control electrode connected to an inverse of the second control signal.

21. A buffer circuit according to Claim 20, the second logic gate further comprising a fifth transistor connected in series with the second transistor between the first transistor and the reference voltage.

22. A buffer circuit according to Claim 13 wherein the reference voltage comprises a ground voltage.

23. A buffer circuit according to Claim 13 wherein the first logic gate comprises a NAND gate and wherein the second logic gate comprises a NOR gate.

24. A buffer circuit according to Claim 13 wherein the plurality of

serially connected transistors in the path between the first output node and the reference voltage are NMOS transistors, and wherein the plurality of serially connected transistors in the path between the second output node and the reference voltage are NMOS transistors.

25. A buffer circuit comprising;

an output terminal;

a pull-up transistor connected between the output terminal and a supply voltage, wherein the pull-up transistor pulls the output terminal up to the supply voltage responsive to a pull-up control signal;

a pull-down transistor connected between the output terminal and a reference voltage, wherein the pull-down transistor pulls the output terminal down to the reference voltage responsive to a pull-down control signal;

a first logic gate configured to generate the pull-up control signal at a first output node responsive to a control signal and a data signal, and wherein the first logic gate includes first and second transistors connected in parallel between the supply voltage and the first output node and third and fourth transistors connected in parallel between the first output node and the reference voltage; and

a second logic gate configured to generate the pull-down control signal at a second output node responsive to the data signal and an inverse of the control signal.

26. A buffer circuit according to Claim 25 wherein the first and second transistors comprises PMOS transistors and wherein the third and fourth transistors comprise NMOS transistors.

27. A buffer circuit according to Claim 26 wherein a first control electrode of the first transistor is connected to the data signal, wherein a second control electrode of the second transistor is connected to the control signal, wherein a third control electrode of the third transistor is connected to the data signal, and wherein a fourth control electrode of the

fourth transistor is connected to the reference voltage.

28. A buffer circuit according to Claim 27 wherein the first logic gate further comprises a fifth transistor connected in parallel with the first and second transistors between the supply voltage and the first output node, wherein the fifth transistor comprises a PMOS transistor having a control electrode connected to a second control signal.

29. A buffer circuit according to Claim 25 wherein the first logic gate further comprises a fifth transistor coupled in series between the supply voltage and the first and second transistors, and a sixth transistor coupled in series between the reference voltage and the third and fourth transistors.

30. A buffer circuit according to Claim 25 wherein the second logic gate includes fifth and sixth transistors connected in parallel between the supply voltage and the second output node and seventh and eighth transistors connected in parallel between the second output node and the reference voltage.

31. A buffer circuit according to Claim 30 wherein first and second and fifth and sixth transistors comprise PMOS transistors, and wherein the third and fourth and seventh and eighth transistors comprise NMOS transistors.

32. A buffer circuit according to Claim 31 wherein a first control electrode of the first transistor is connected to the data signal, wherein a second control electrode of the second transistor is connected to the control signal, wherein a third control electrode of the third transistor is connected to the data signal, wherein a fourth control electrode of the fourth transistor is connected to the reference voltage, wherein a fifth control electrode of the fifth transistor is connected to the data signal,

wherein a sixth control electrode of the sixth transistor is connected to the supply voltage, wherein a seventh control electrode of the seventh transistor is connected to the data signal, and wherein an eighth control electrode of the eighth transistor is connected to the inverse of the control signal.

33. A buffer circuit comprising;

an output terminal;

a pull-up transistor connected between the output terminal and a supply voltage, wherein the pull-up transistor pulls the output terminal up to the supply voltage responsive to a pull-up control signal;

a pull-down transistor connected between the output terminal and a reference voltage, wherein the pull-down transistor pulls the output terminal down to the reference voltage responsive to a pull-down control signal;

a first logic gate which configured to generate the pull-up control signal at a first output node responsive to a control signal and a data signal; and

a second logic gate configured to generates the pull-down control signal at a second output node responsive to the data signal and an inverse of the control signal, and wherein the second logic gate includes first and second transistors connected in parallel between the supply voltage and the second output node and third and fourth transistors connected in parallel between the second output node and the reference voltage.

34. A buffer circuit according to Claim 33 wherein the first and second transistors comprises PMOS transistors and wherein the third and fourth transistors comprise NMOS transistors.

35. A buffer circuit according to Claim 34 wherein a first control electrode of the first transistor is connected to the data signal, wherein a second control electrode of the second transistor is connected to the supply

voltage, wherein a third control electrode of the third transistor is connected to the data signal, and wherein a fourth control electrode of the fourth transistor is connected to the inverse of the control signal.

36. A buffer circuit according to Claim 35 wherein the second logic gate further comprises a fifth transistor connected in parallel with the first and second transistors between the supply voltage and the second output node, wherein the fifth transistor comprises a PMOS transistor having a control electrode connected to an inverse of a second control signal.

37. A buffer circuit according to Claim 33 wherein the second logic gate further comprises a fifth transistor coupled in series between the supply voltage and the first and second transistors, and a sixth transistor coupled in series between the reference voltage and the third and fourth transistors.

38. A buffer circuit according to Claim 33 wherein the first logic gate includes fifth and sixth transistors connected in parallel between the supply voltage and the first output node and seventh and eighth transistors connected in parallel between the first output node and the reference voltage.

39. A buffer circuit according to Claim 38 wherein first and second and fifth and sixth transistors comprise PMOS transistors, and wherein the third and fourth and seventh and eighth transistors comprise NMOS transistors.

40. A buffer circuit according to Claim 39 wherein a first control electrode of the first transistor is connected to the data signal, wherein a second control electrode of the second transistor is connected to the supply voltage, wherein a third control electrode of the third transistor is connected

to the data signal, wherein a fourth control electrode of the fourth transistor is connected to an inverse of the control signal, wherein a fifth control electrode of the fifth transistor is connected to the data signal, wherein a sixth control electrode of the sixth transistor is connected to the control signal, wherein a seventh control electrode of the seventh transistor is connected to the data signal, and wherein an eighth control electrode of the eighth transistor is connected to the reference voltage.

41. An output buffer circuit comprising:

a pull-up transistor which pulls up an output terminal in response to a pull-up control signal;

a pull-down transistor which pulls down the output terminal in response to a pull-down control signal;

a NAND gate which receives at least one control signal and data and generates the pull-up control signal; and

a NOR gate which receives an inverted signal of the control signal and the data and generates the pull-down control signal,

wherein the number of PMOS transistors present along the path of first supply voltage to an output terminal of the NAND gate is equivalent to the number of PMOS transistors present along the path of the first supply voltage to an output terminal of the NOR gate, and the number of NMOS transistors present along the path of a second supply voltage to an output terminal of the NAND gate is equivalent to the number of NMOS transistors present along the path of the second supply voltage to an output terminal of the NOR gate.

42. The output buffer circuit of claim 41, wherein the NAND gate comprises:

a first PMOS transistor which has a source to which the first supply voltage is applied and a gate to which the second supply voltage is applied;

a second PMOS transistor which has a source connected to a drain of the first PMOS transistor, a gate to which the data is input, and a drain connected to the output terminal of the NAND gate;

a third PMOS transistor which has a source connected to the drain of the first PMOS transistor, a gate to which the control signal is applied, and a drain connected to the output terminal of the NAND gate;

a first NMOS transistor which has a drain connected to the output terminal of the NAND gate and a gate to which the data is input; and

a second NMOS transistor which has a drain connected to a source of the first NMOS transistor, a gate to which the control signal is applied, and a source to which the second supply voltage is applied.

43. The output buffer circuit of claim 41, wherein the NOR gate includes:

a first PMOS transistor which has a source to which the first supply voltage is applied and a gate to which the inverted signal of the control signal is applied;

a second PMOS transistor which has a source connected to a drain of the first PMOS transistor, a gate to which the data is input, and a drain connected to the output terminal of the NOR gate;

a first NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the inverted signal of the control signal is applied;

a second NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the data is input; and

a third NMOS transistor which has a drain connected to sources of the first and second NMOS transistors, a gate to which the first supply voltage is applied, and a source to which the second supply voltage is applied.

44. The output buffer circuit of claim 42, wherein the NAND gate further comprises a third NMOS transistor which has a drain connected to

the output terminal of the NAND gate, a gate to which the second supply voltage is applied, and a source connected to the source of the first NMOS transistor.

45. The output buffer circuit of claim 43, wherein the NOR gate further comprises a third PMOS transistor which has a source connected to the drain of the first PMOS transistor, a gate to which the first supply voltage is applied, and a drain connected to the output terminal of the NOR gate.

46. The output buffer circuit of claim 41, wherein the NAND gate comprises:

a first PMOS transistor which has a source to which the first supply voltage is applied and a gate to which the second supply voltage is applied;

a second PMOS transistor which has a source connected to the drain of the first PMOS transistor and a gate to which the second supply voltage is applied;

a third PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which the data is input, and a drain connected to the output terminal of the NAND gate;

a fourth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which a first control signal is applied, and a drain connected to the output terminal of the NAND gate;

a fifth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which a second control signal is applied, and a drain connected to the output terminal of the NAND gate;

a first NMOS transistor which has a drain connected to the output terminal of the NAND gate and a gate to which the data is input;

a second NMOS transistor which has a drain connected to a source of the first NMOS transistor and a gate to which the first control signal is applied; and

a third NMOS transistor which has a drain connected to a source of the second NMOS transistor, a gate to which the second control signal is applied, and a source to which the second supply voltage is applied.

47. The output buffer circuit of claim 41, wherein the NOR gate comprises:

a first PMOS transistor which has a source to which the first supply voltage is applied and a gate to which the data is input;

a second PMOS transistor which has a source connected to a drain of the first PMOS transistor and a gate to which an inverted signal of the first control signal is applied;

a third PMOS transistor which has a source connected to a drain of the second PMOS transistor, a gate to which an inverted signal of the second control signal is applied, and a drain connected to the output terminal of the NOR gate;

a first NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the data is input;

a second NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which an inverted signal of the first control signal is applied;

a third NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which an inverted signal of the second control signal is applied;

a fourth NMOS transistor which has a drain connected to sources of the first through third NMOS transistors and a gate to which the first supply voltage is applied; and

a fifth NMOS transistor which has a drain connected to a source of the fourth NMOS transistor, a gate to which the first supply voltage is applied, and a source to which the second supply voltage is applied.

48. The output buffer circuit of claim 46, wherein the NAND gate comprises a fourth NMOS transistor which has a drain connected to the

output terminal of the NAND gate, a gate to which the second supply voltage is applied, and a source connected to the source of the first NMOS transistor; and

a fifth NMOS transistor which has a drain connected to the output terminal of the NAND gate, a gate to which the second supply voltage is applied, and a source connected to the source of the first NMOS transistor.

49. The output buffer circuit of claim 47, wherein the NOR gate further comprises:

a fourth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which the first supply voltage is applied, and a drain connected to the output terminal of the NOR gate; and

a fifth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which the first supply voltage is applied, and a drain connected to the output terminal of the NOR gate.

50. An output buffer circuit comprising:

a pull-up transistor which pulls up an output terminal in response to a pull-up control signal;

a pull-down transistor which pulls down the output terminal in response to a pull-down control signal;

a NAND gate which receives a control signal and data and generates the pull-up control signal; and

a NOR gate which receives an inverted signal of the control signal and the data and generates the pull-down control signal,

wherein the NAND gate comprises:

a first PMOS transistor which has a source to which a first supply voltage is applied and a gate to which a second supply voltage is applied;

a second PMOS transistor which has a source connected to a drain of the first PMOS transistor, a gate to which the data is input, and a drain connected to an output terminal of the NAND gate;

a third PMOS transistor which has a source connected to the drain of the first PMOS transistor, a gate to which the control signal is applied, and a drain connected to the output terminal of the NAND gate;

a first NMOS transistor which has a drain connected to the output terminal of the NAND gate and a gate to which the data is input; and

a second NMOS transistor which has a drain connected to a source of the first NMOS transistor, a gate to which the control signal is applied, and a source to which the second supply voltage is applied, and

the NOR gate comprises:

a first PMOS transistor which has a source to which first supply voltage is applied and a gate to which the inverted signal of the control signal is applied;

a second PMOS transistor which has a source connected to the drain of the first PMOS transistor, a gate to which the data is input, and a drain connected to the output terminal of the NAND gate;

a first NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the inverted signal of the control signal is applied;

a second NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the data is applied; and

a third NMOS transistor which has a drain connected to sources of the first and second NMOS transistors, a gate to which the first supply voltage is applied, and a source to which the second supply voltage is applied.

51. The output buffer circuit of claim 50, wherein the NAND gate further comprises a third NMOS transistor which has a drain connected to the output terminal of the NAND gate, a gate to which the second supply voltage is applied, and a source connected to the source of the first NMOS transistor.

52. The output buffer circuit of claim 50, wherein the NOR gate further comprises a third NMOS transistor which has a source connected to the drain of the first PMOS transistor, a gate to which the first supply voltage is applied, and a drain connected to the output terminal of the NOR gate.

53. An output buffer circuit comprising:

a pull-up transistor which pulls up an output terminal in response to a pull-up control signal;

a pull-down transistor which pulls down the output terminal in response to a pull-down control signal;

a NAND gate which receives a first control signal, a second control signal, and data and generates the pull-up control signal; and

a NOR gate which receives an inverted signal of the first control signal, an inverted signal of the second control signal and the data, and generates the pull-down control signal,

wherein the NAND gate comprises:

a first PMOS transistor which has a source to which a first supply voltage is applied and a gate to which a second supply voltage is applied;

a second PMOS transistor which has a source connected to a drain of the first PMOS transistor and a gate to which the second supply voltage is applied;

a third PMOS transistor which has a source connected to a drain of the second PMOS transistor, a gate to which the data is input, and a drain connected to the output terminal of the NAND gate;

a fourth PMOS transistor which has a source connected to a drain of the second PMOS transistor, a gate to which the first control signal is applied, and a drain connected to the output terminal of the NAND gate;

a fifth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which the second control signal is applied, and a drain connected to the output terminal of the NAND gate;

a first NMOS transistor which has a drain connected to the output terminal of the NAND gate and a gate to which the data is input;

a second NMOS transistor which has a drain connected to a source of the first NMOS transistor and a gate to which the first control signal is applied; and

a third NMOS transistor which has a drain connected to a source of the second NMOS transistor, a gate to which the second control signal is applied, and a source to which the second supply voltage is applied, and

the NOR gate comprises:

a first PMOS transistor which has a source to which the first supply voltage is applied and a gate to which the data is input;

a second PMOS transistor which has a source connected to a drain of the first PMOS transistor and a gate to which an inverted signal of the first control signal is applied;

a third PMOS transistor which has a source connected to a drain of the second PMOS transistor, a gate to which an inverted signal of the second control signal is applied, and a drain connected to the output terminal of the NOR gate;

a first NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the data is input;

a second NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the inverted signal of the first control signal is applied;

a third NMOS transistor which has a drain connected to the output terminal of the NOR gate and a gate to which the inverted signal of the second control signal is applied;

a fourth NMOS transistor which has a drain connected to sources of the first through third NMOS transistors and a gate to which the first supply voltage is applied; and

a fifth NMOS transistor which has a drain connected to a source of the fourth NMOS transistor, a gate to which the first supply voltage is applied, and a source to which the second supply voltage is applied.

54. The output buffer circuit of claim 53, wherein the NAND gate further comprises:

a fourth NMOS transistor which has a drain connected to the output terminal of the NAND gate, a gate to which the second supply voltage is applied, and a source connected to the source of the first NMOS transistor; and

a fifth NMOS transistor which has a drain connected to the output terminal of the NAND gate, a gate to which the second supply voltage is applied, and a source connected to the source of the first NMOS transistor.

55. The output buffer circuit of claim 53, wherein the NOR gate comprises:

a fourth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which the first supply voltage is applied, and a drain connected to the output terminal of the NOR gate; and

a fifth PMOS transistor which has a source connected to the drain of the second PMOS transistor, a gate to which the first supply voltage is applied, and a drain connected to the output terminal of the NOR gate.